REMARKS

Claims 1- 19 were pending in this application and rejected by the Examiner. Claims 1, 3, 4 and 7 have been amended. Claims 2, 5-6, 8, 11-12, and 16-19 have been canceled. New claims 20-24 have been added by this amended. Claims 1, 3, 4, 7, 9, 10, 13-15, and 20-24 are currently pending. Applicants reserve the right to pursue the original claims and other claims in this application and in other applications.

The drawings stand objected to for failing to show the claim 10 NMOS sample and hold and reset transistors. Claim 7 from which claim 10 depends has been amended to recite a NMOS frame shutter. FIG. 4 shows the an NMOS frame shutter having NMOS transistors. Accordingly, Applicants respectfully request that the objection to the drawings be withdrawn.

The drawings stand objected to for failing to label FIGS. 1-2 as "Prior Art." Applicants respectfully submit that FIG 1 is not prior art, but Applicants believe FIG 2 to be prior art. The label "Prior Art" has been added to FIG. 2 of the replacement drawing sheet attached to this amendment. No new matter has been added. Applicants respectfully request that the objection to FIG. 1 be withdrawn, and further submit that the objection to FIG 2 is now moot.

Claims 11 and 12 stand rejected under 35 U.S.C. § 112, first paragraph, as failing to comply with the enablement requirement. Applicants have canceled claims 11 and 12. Accordingly, Applicants submit that the rejections of claims 11 and 12 are moot.

Claims 18 and 19 stand rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicants regard as the invention. Claims 18 and 19 have been canceled. Applicants submit that the Examiner's indefiniteness rejection is moot.

Claims 1, 5, and 6 stand rejected as being anticipated by Gowda et al., US Patent No. 5,898,168 (hereinafter "Gowda"). Claims 5 and 6 have been canceled, thus the rejection of these claims is now moot. Regarding amended Claim 1, the rejection is respectfully traversed and reconsideration is respectfully requested. Gowda teaches increasing the area available to the light sensitive areas of an imager by eliminating the need for a large MOSFET row select transistor in each of the image cells. Although Gowda discloses the use of a shutter transistor, Gowda does not disclose the frame shutter of the present invention. Gowda discloses an array of shutter transistors that are collectively activated by an external switch. (Gowda at Col. 10, l. 45 – Col. 11, l. 21). Each shutter transistor is connected in series to a transistor 22, and stores charge until the corresponding image cell (pixel) is ready for row by row readout via transistor 22 (which performs a row select function). (Gowda at Col. 10, l. 45 – Col. 11, l. 21; Fig. 15). Gowda does not disclose a frame shutter in a P-well as recited in Claim 1. Applicants respectfully submit that for at least the reasons set forth above, Claim 1 is allowable over Gowda.

Claims 7-9, 11 and 12 stand rejected as being anticipated by prior art Figure 2. Claims 8, 11 and 12 have been canceled, and thus the rejection of these claims is now moot. Regarding Amended Claim 7 and Claim 9, the rejection is respectfully traversed and reconsideration is respectfully requested. Applicants submit that Claim 7 and Claim 9 are allowable over Figure 2. Figure 2 does not disclose a pinned photodiode as recited in Claim 7. For at least the reasons set forth above, claim 7 and claim 9, which depends from claim 7, are allowable over Figure 2.

Claims 2-4, 7-9, 11 and 12 stand rejected under 35 U.S.C. § 103(a) as being obvious over Gowda in view of Liu et al., US Patent No. 6,300,632 (hereinafter "Liu"). Claims 2, 8, 11 and 12 have been canceled, and therefore Applicants submit that the rejection of these claims is moot. Regarding claims 3, 4, 7 and 9, Applicants respectfully

traverse the rejections and request reconsideration. Liu discloses the use of heat-balancing techniques (Liu at Col. 2, ll. 27-46) in an imager using a heater device for providing controllable heat. (Liu at Col. 2, ll. 47-62). Liu states that the imager comprises a plane of microelectro-mechanical infrared detectors which each include "a substrate and a sensor positioned in an area thermally isolated from the substrate for sensing temperature and to provide a corresponding temperature signal representing incident power of infrared energy." (Liu at Col. 2, ll. 47-55). The detectors further include "a heater for controllably heating the sensor . . . ." (Liu at Col. 2, ll. 55-57) Gowda teaches that it is desirable to provide an imager that employs as little electronics as possible thereby providing additional area available to enlarge the light sensitive areas of the imager. (Gowda at Col. 1, ll. 28-40, Col. 2, ll. 31-44, Col. 3, ll. 4-11). There is no motivation to combine Lui which teaches the use of additional elements such as a heater, and Gowda which teaches the reduction of imager electronics. For at least the reasons set forth above, claims 3, 4, 7 and 9 are allowable over Gowda in view of Liu.

Claims 13-19 stand rejected under 35 U.S.C. § 103(a) as being obvious over Gowda in view of Kalnitsky et al., United States Patent 6,380,517 (hereinafter the "Kalnitsky"). Claims 16-19 have been canceled, and thus Applicants submit that the rejection of these claims is now moot. The rejection of each claims 13-15 is respectfully traversed and reconsideration is requested. Applicants submit that there is no motivation to combine Gowda and Kalnitsky. According to the Examiner one would be motivated to provide the apparatus of Gowda in view of Kalnitsky to isolate the NMOS circuitry and improve sensitivity. There is, however, no such suggestion in either Gowda or Kalnitsky. Kalnitsky discloses pixel circuitry that is entirely placed into a floating P-well, that is in turn embedded into a N-well on a P-substrate. Kalnitsky does not disclose that the use of a NMOS circuitry in a P-well will improve sensitivity. Rather, Kaltnisky teaches that CCD imager sensors have high sensitivity and fill factor but have weaknesses such as limited readout rates and dynamic range limitations.

(Kalnitsky at Col. 1, ll. 25-30). Kalnitsky further discloses the use of active pixel sensor cells (including a photodiode) to overcome such weaknesses. (Kalnitsky at Col. 1, ll. 31-37). Gowda discloses an imager that comprises a CCD image sensor (or light sensing element such as a photodiode or pinned photo diode) and CMOS electronics, and that is improved by eliminating electronics in the form of a row select transistor. (Gowda at Col. 1, ll. 28-40, Col. 2, ll. 31-44, Col. 3, ll. 4-11). Kalnitsky thus indicates that the image sensors of Gowda have favorable sensitivity characteristics. There is no motivation to combine the teachings of Gowda with those of Kaltnisky in order to isolate the NMOS circuitry and improve sensitivity. Further, there is no suggestion in the references covering how Kalnitsky's disclosure of a P-well should be combined with the teachings of Gowda. Accordingly, for at least the above reasons, withdrawal of the section 103 obviousness rejections of claims 13-15 is respectfully requested.

Claims 20-22 include subject matter disclosed in FIGs. 4 and 5, and Claims 23-24 include subject matter disclosed in FIG. 3. Applicants submit that Claims 20-24 are allowable over the prior art.

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to withdraw the outstanding rejection of the claims and to pass this application to issue.

Dated: September 29, 2003

Respectfully submitted,

By _____

Thomas J. D'Amico
Registration No.: 28,371
DICKSTEIN SHAPIRO MORIN &
OSHINSKY LLP
2101 L Street NW
Washington, DC 20037-1526
(202) 785-9700
Attorneys for Applicants